

publ. 2385100

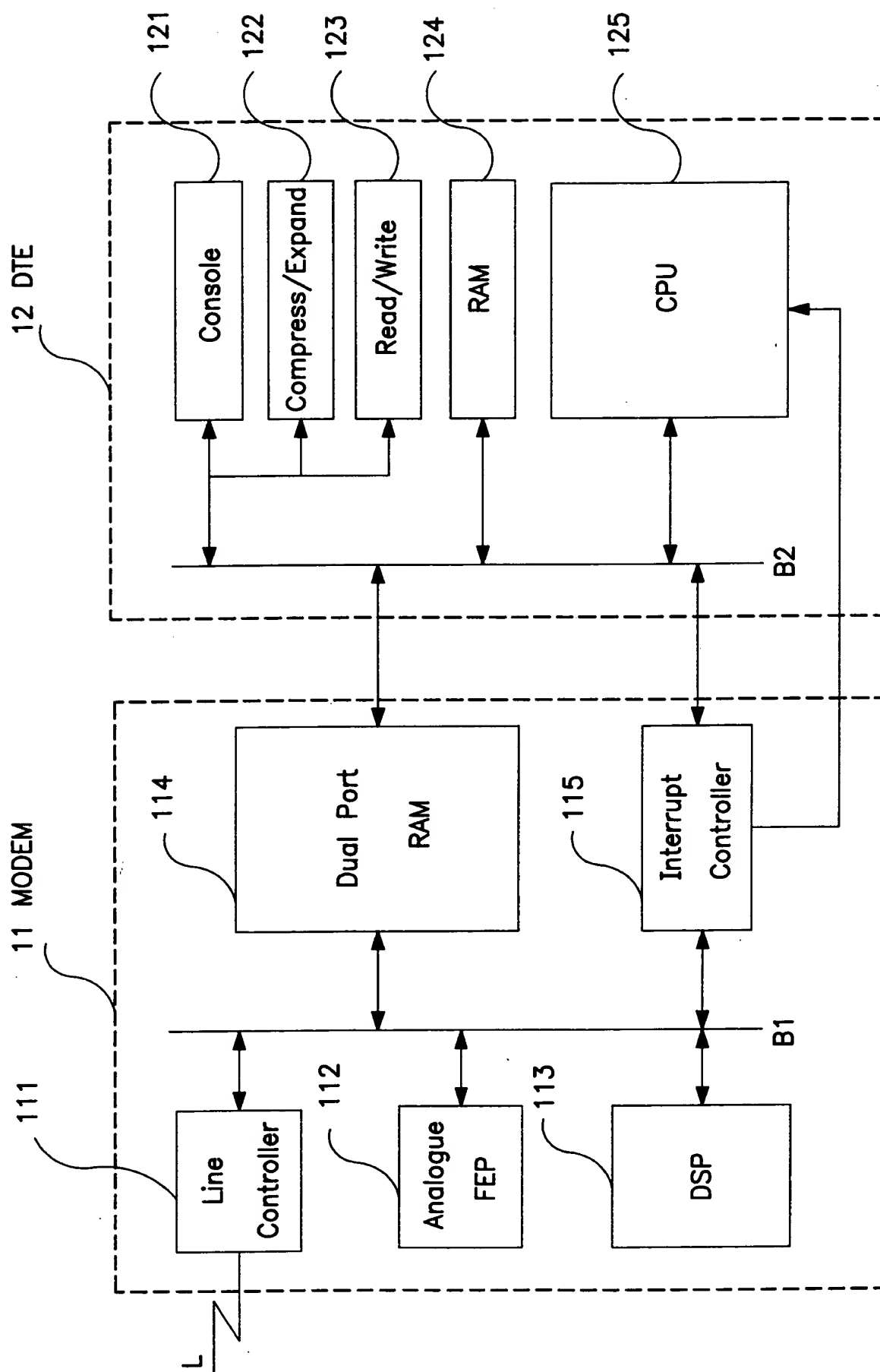


FIG. 1

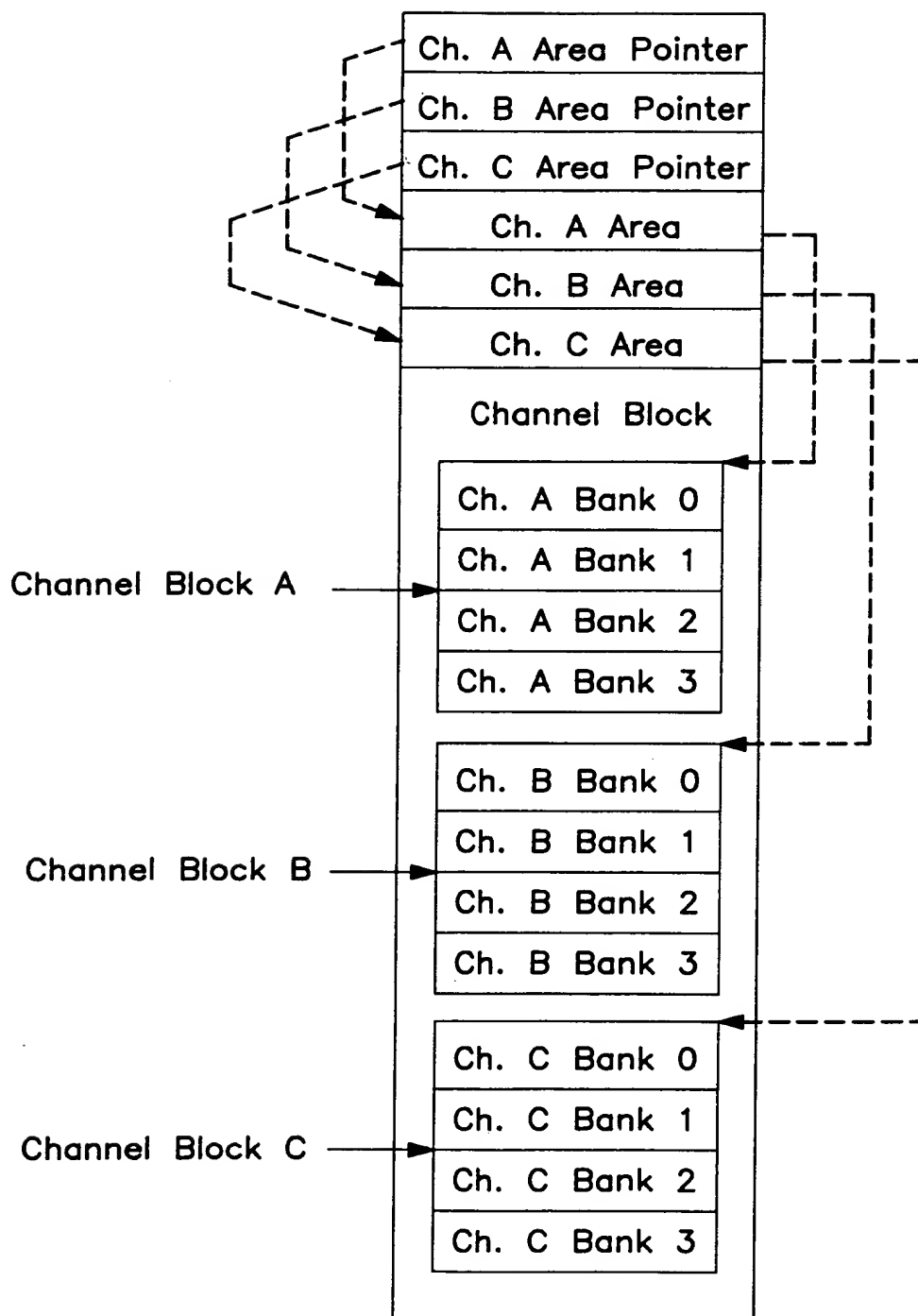
[illegible]

FIG. 2

[illegible]FIG. 3

7	6	5	4	3	2	1	0

0: receiving mode

FIG. 4

DocId: 33333333

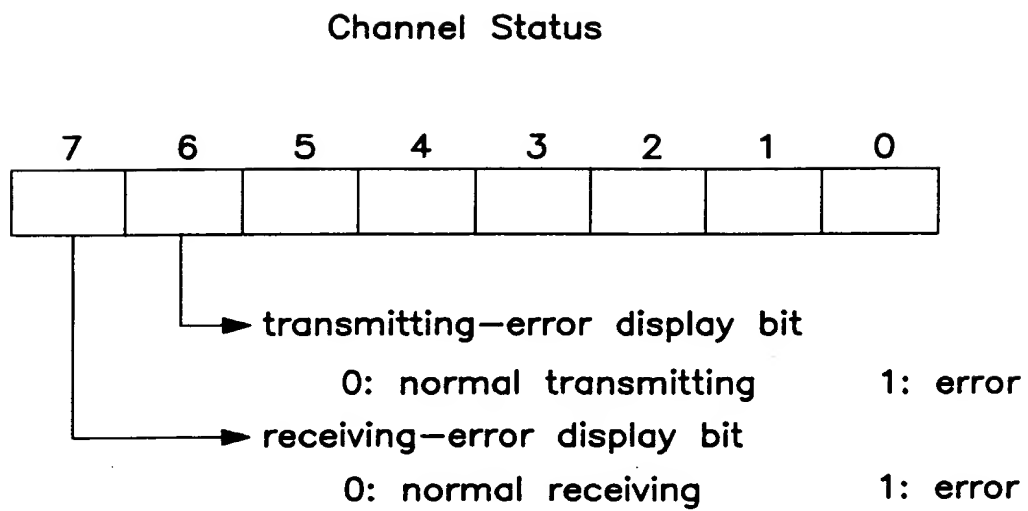


FIG. 5

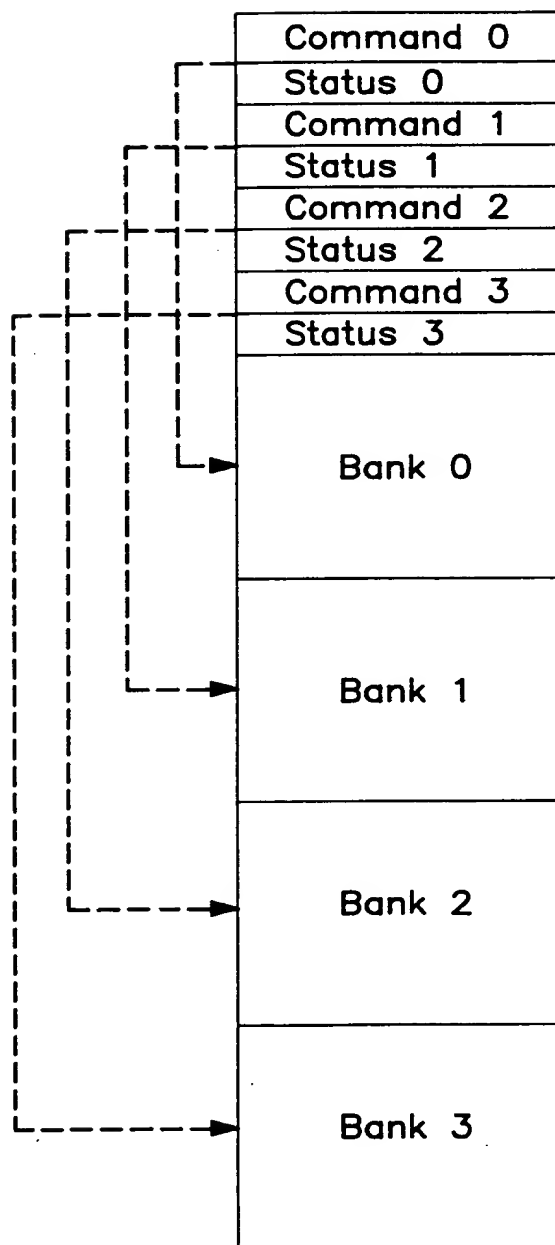
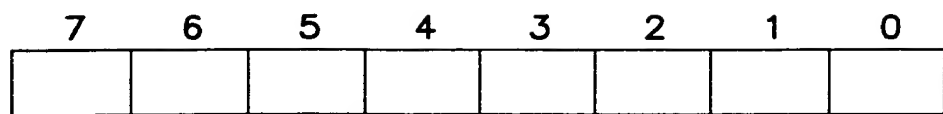


FIG. 6

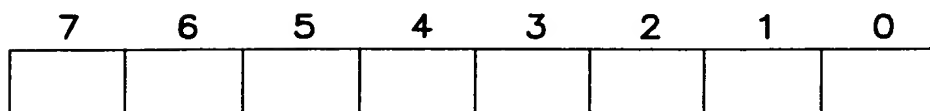
Channel 0



End-instruction bit to each channel
 0: not end
 1: end

FIG. 7

Status 0



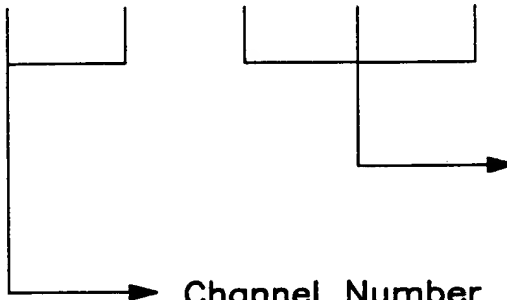
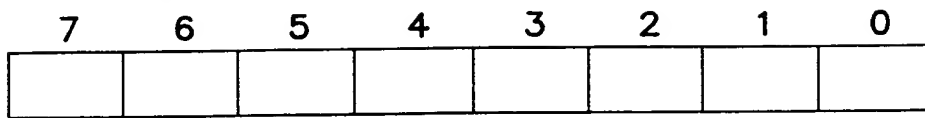
FCS NG
 0: FCS OK
 1: FCS NG

Abort occurs
 0: no abort in this bank
 1: abort exists in this bank

Data Full/Empty display bit
 0: Read end = Write enable
 1: Write end = Read enable

FIG. 8

Transmitting Interrupt Status



Channel Number

00: Channel A

01: Channel B

10: Channel C

Bank Number

000: bank 0

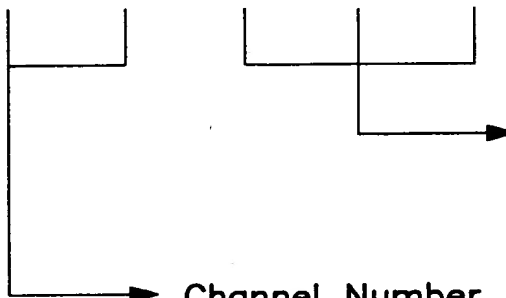
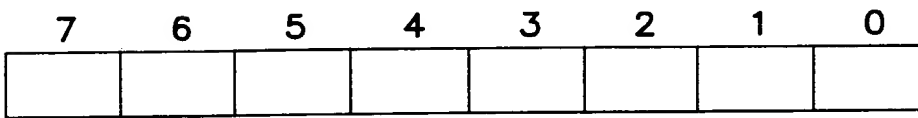
001: bank 1

010: bank 2

011: bank 3

FIG. 9

Receiving Interrupt Status



Channel Number

00: Channel A

01: Channel B

10: Channel C

Bank Number

000: bank 0

001: bank 1

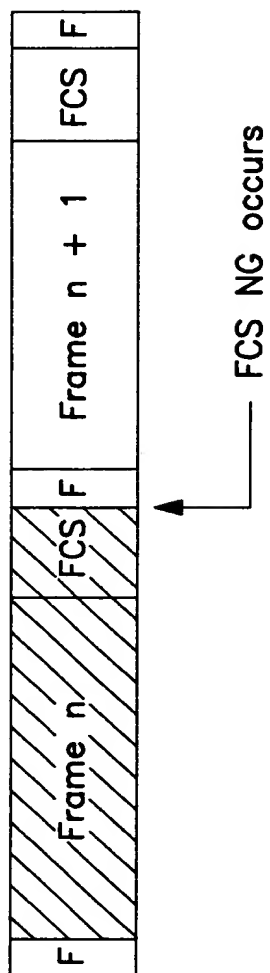
010: bank 2

011: bank 3

110: FCS error

111: Abort

FIG. 10



II

Bank 0

Frame $n - 1$

Bank 1

Frame n

Bank 2

Bank 3

Bank 0
Frame $n - 1$
Bank 1
Frame $n + 1$
Bank 2
Frame $n + 2$
Bank 3

The diagram shows a sequence of frames in a bit stream. The first frame, labeled "Frame n", starts with a flag 'F' followed by a hatched area representing the frame data. An arrow labeled "abort occurs" points to the middle of this hatched area. Following the abort, the bit stream continues with an empty space, then an FCS field, a flag 'F', and the start of the next frame, labeled "Frame n + 1". This next frame also includes an FCS field and a flag 'F'.

FIG. 13

Bank 0

Frame n - 1

Bank 1

Frame n

Bank 2

Bank 3

Bank 0
Frame $n - 1$
Bank 1
Frame $n + 1$
Bank 2
Bank 3

FIG. 14 (B)

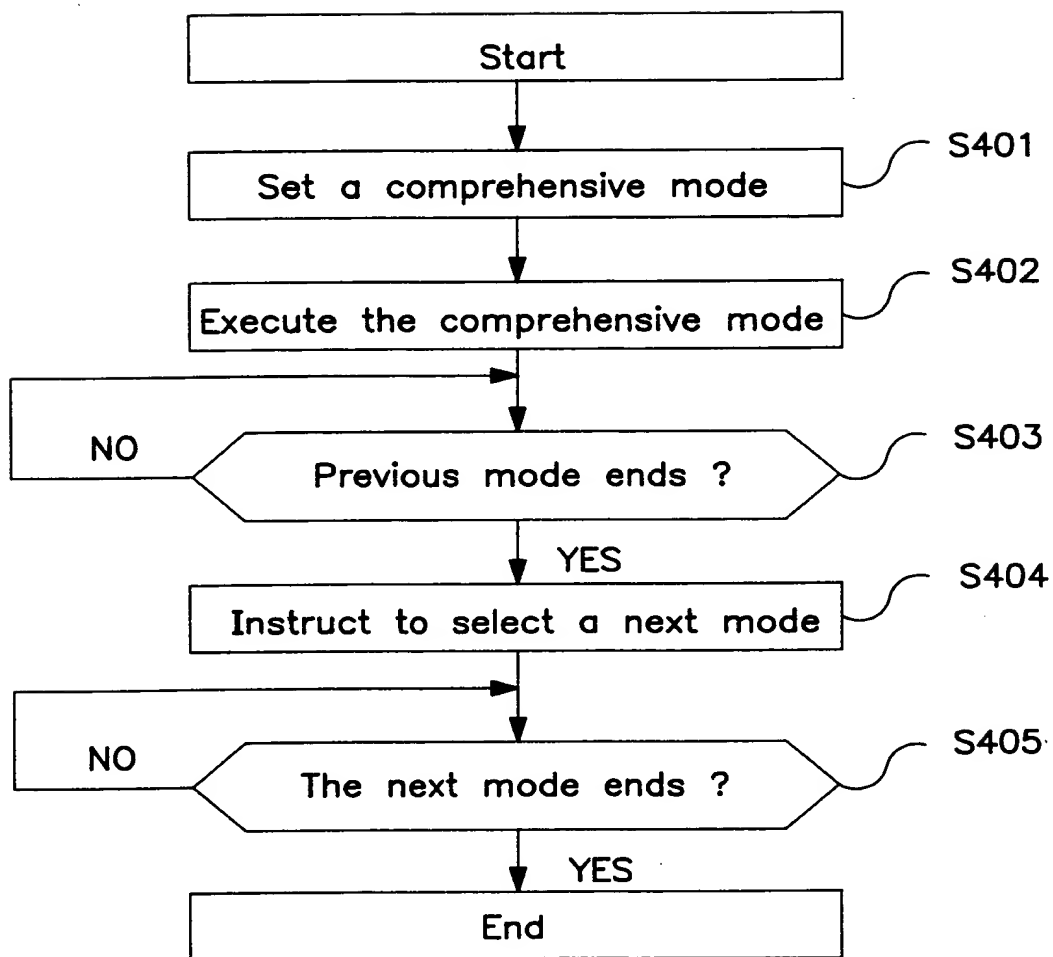


FIG. 15

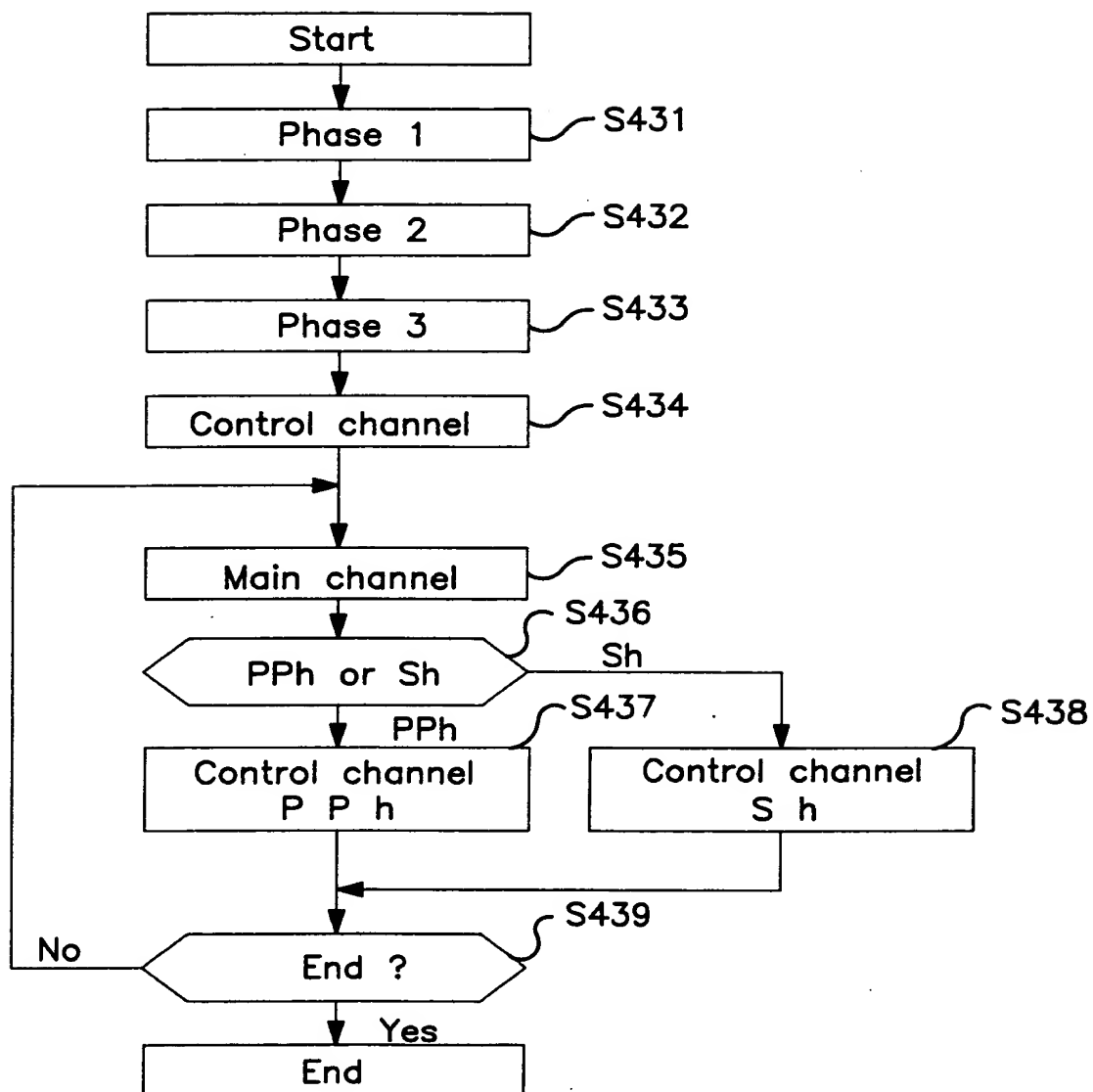


FIG. 16

Mode Switching by RCP Detection

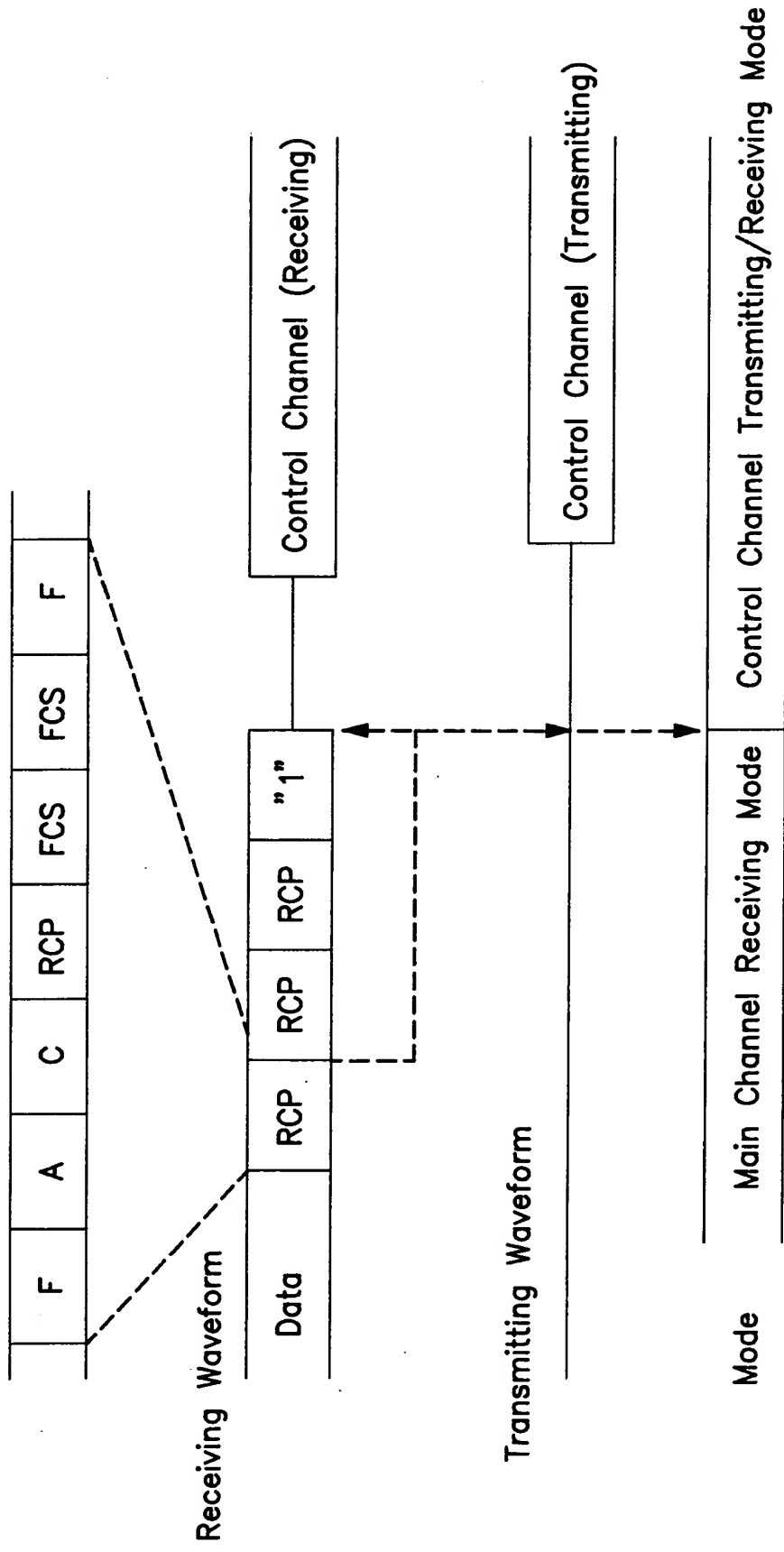


FIG. 17

Mode Switching by Control-channel-ending-signal

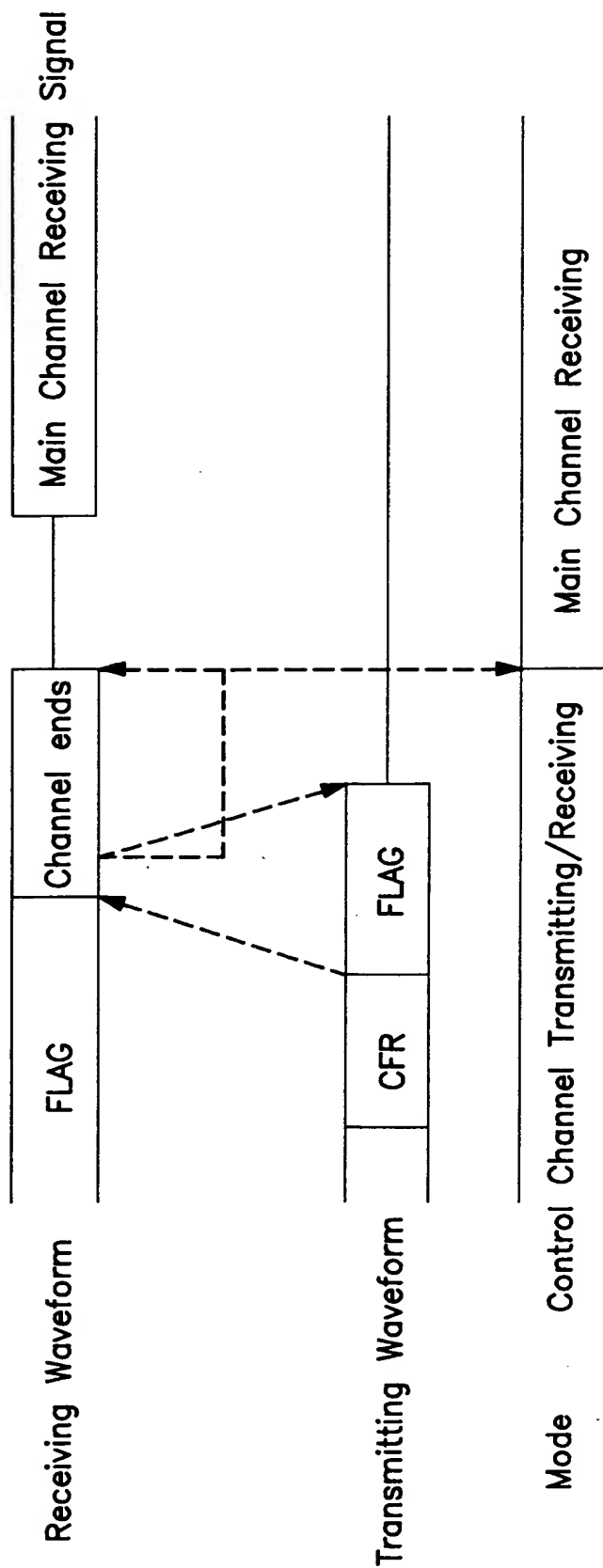


FIG. 18

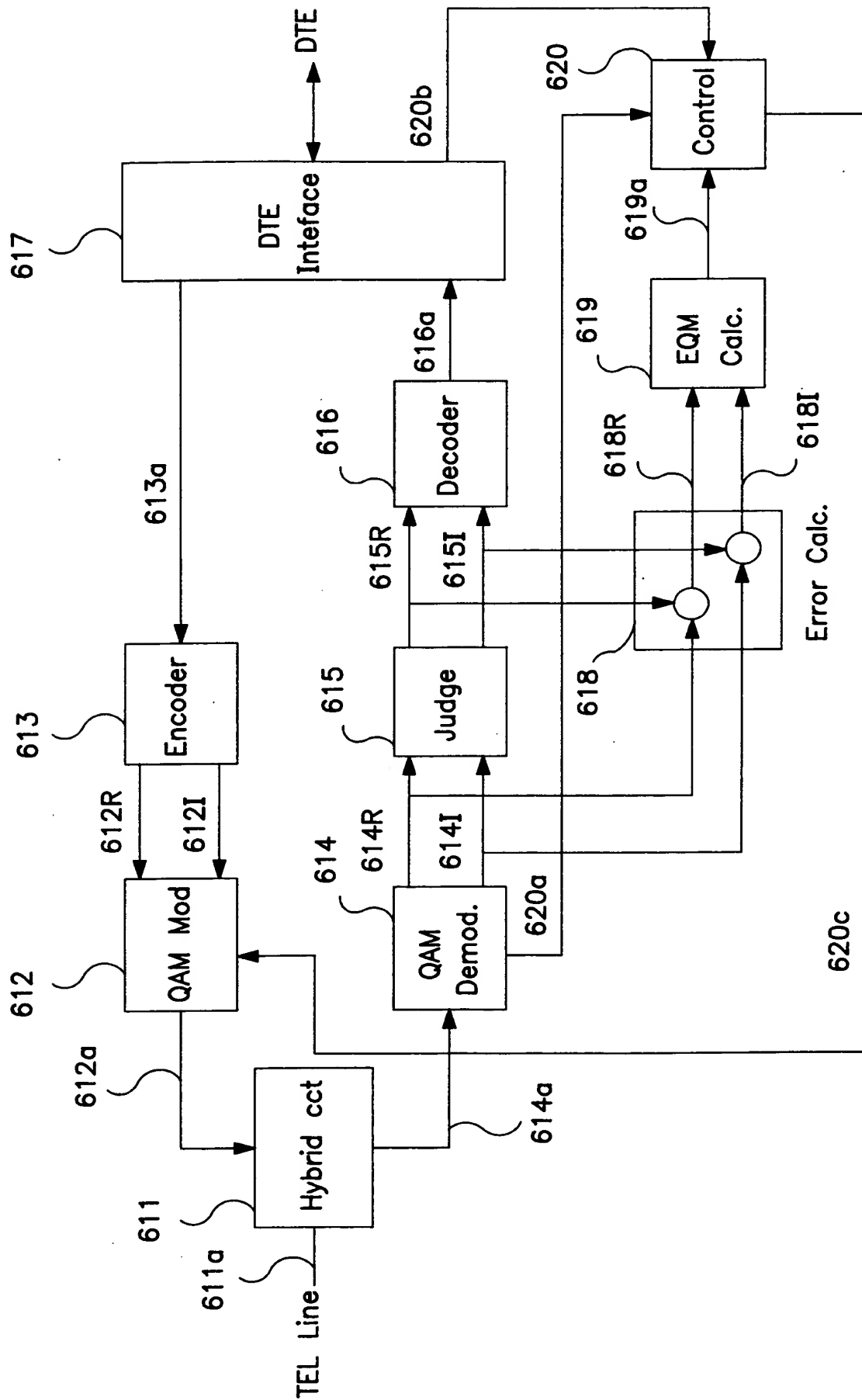


FIG. 19

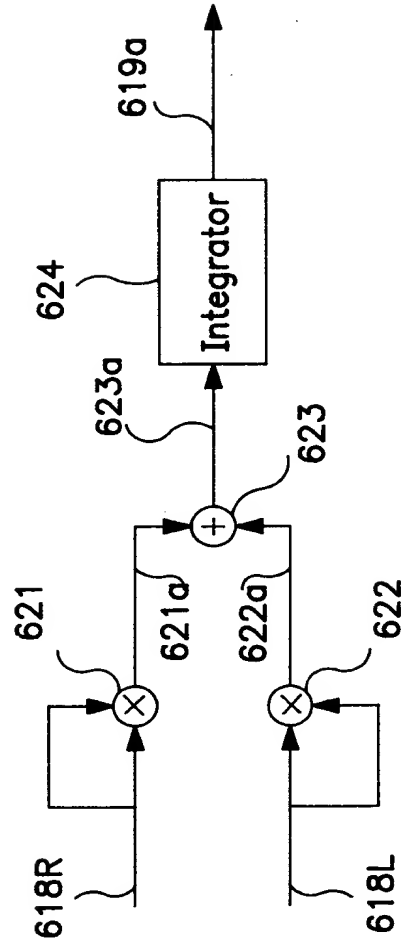


FIG. 20

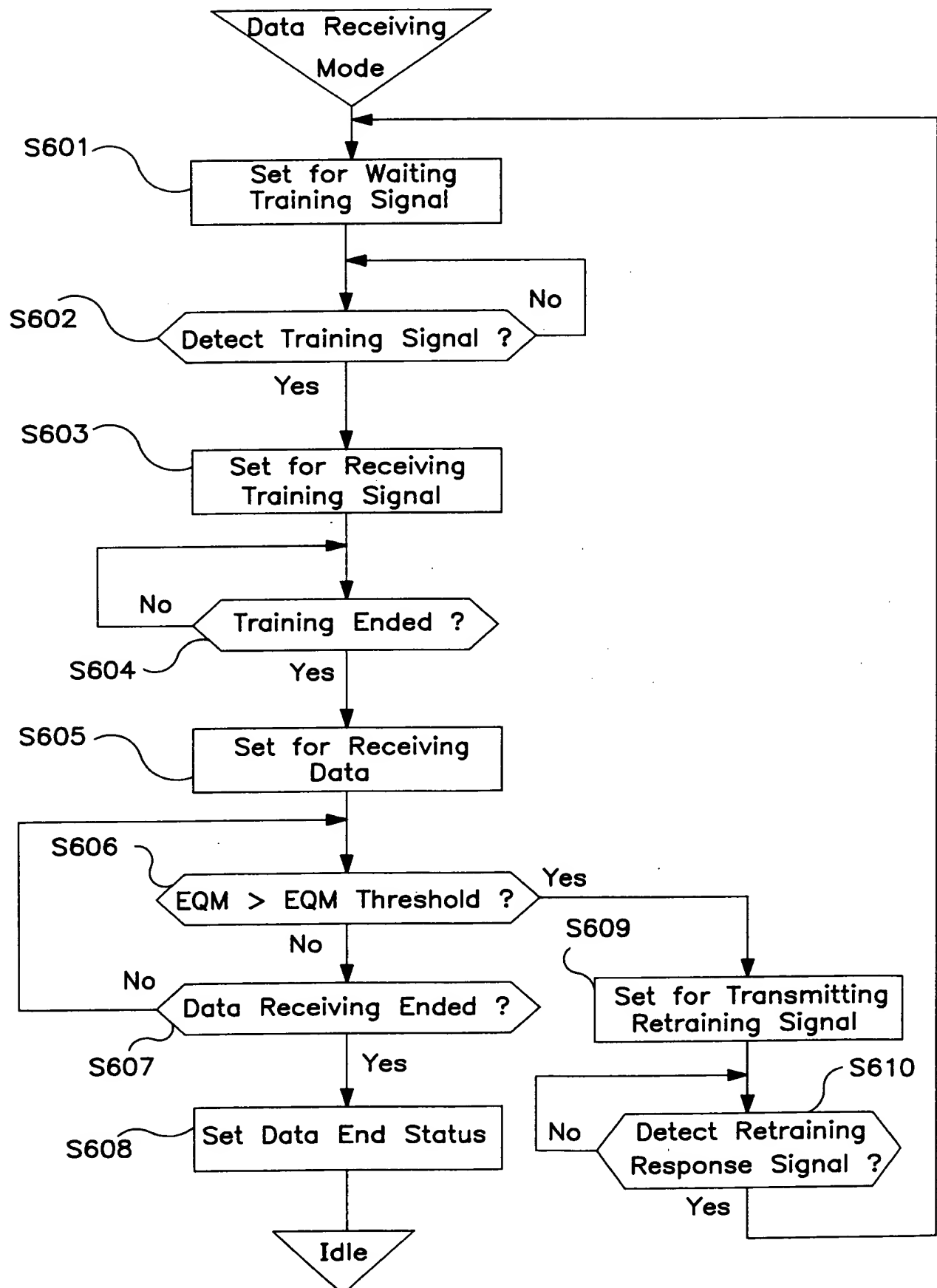
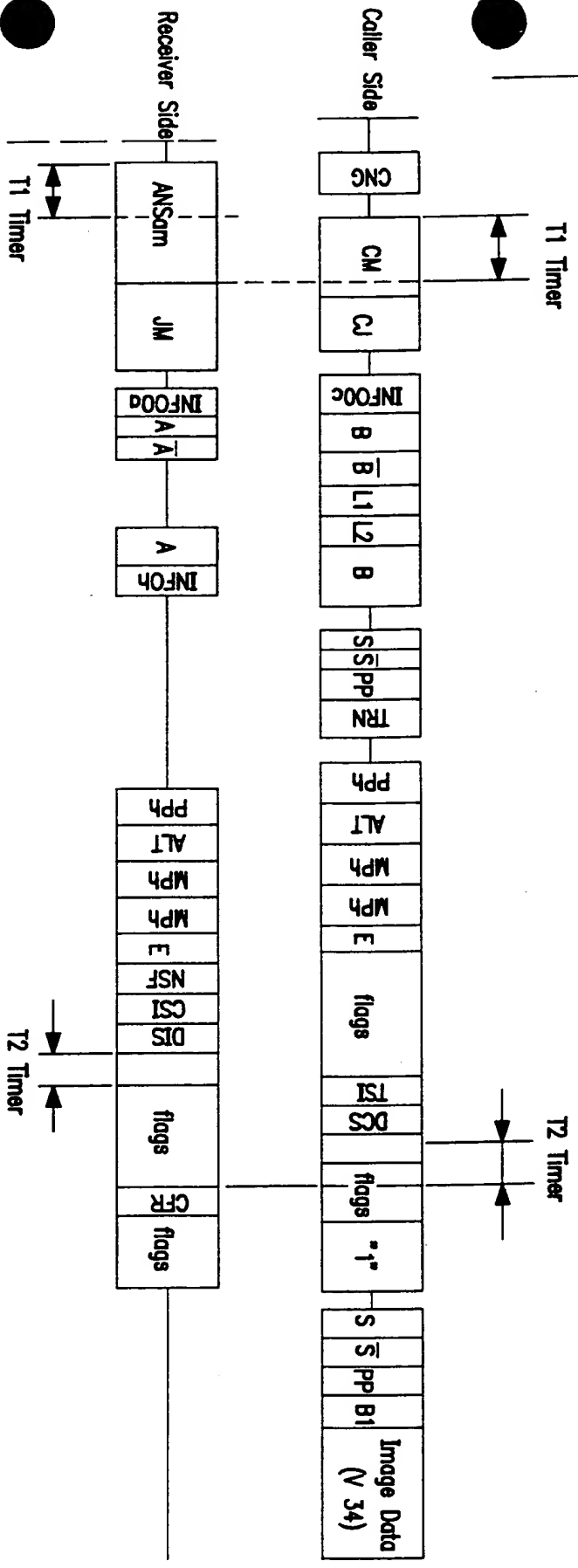


FIG. 21

Transmitting Mode

V34. Facsimile Start Up Procedure

V34. Caller Side Mode



V34. Receiver Side Mode

FIG. 22

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